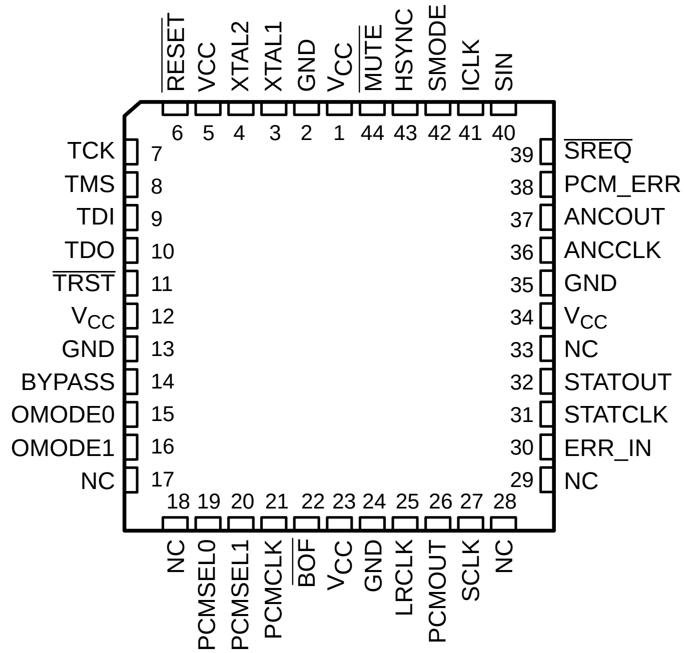
- **Single-Chip ISO-MPEG (Layers 1 and 2) Audio Decoder**
- **Decodes Mono, Dual, Stereo, and Joint-Stereo Modes**
- **Supports All MPEG Sampling and Data Rates**
- **Does Not Require a Host Microprocessor for Initialization or Operation**
- **Accepts SCR and Audio PTS and Provides Automatic Synchronization**
- **Provides Status Information at Beginning of Every Frame**
- **Interfaces Directly to the TMS320AV220 Video Decoder**
- **Hardware Frame Synchronization Input**
- **Supports 16- and 18-Bit PCM Data**
- **Recovers and Outputs All Ancillary Data**
- **PCMCLK-to-Input-Data-Rate Synchronization Signal**
- **IEEE Standard 1149.1 (JTAG) Compatible**
- **Low-Power Submicron CMOS EPIC™ Technology, Fully TTL Compatible**

FN PACKAGE
(TOP VIEW)



description

The Texas Instruments TMS320AV120 is a low-cost, stand-alone MPEG audio decoder. It implements the ISO-MPEG audio decompression algorithm for layers 1 and 2. MPEG-compliant audio data streams at any of the valid MPEG data and sampling rates are accepted, producing decompressed PCM audio output. Mono, dual, stereo, and joint-stereo modes are supported. The serial-output data stream is suitable for direct input to most commercially available one-bit D/A converters.

The design intent is to produce a simple, “plug and play” audio decoder that does not require a host microprocessor for initialization and/or operation. The input is in MPEG audio frame format with provisions for audio/video synchronization. It is a single-chip solution with no provision or need for external buffer memory. The input data rate should match the actual compressed audio bit rate, although the ’AV120 has an input buffer to absorb short-term input bit rate variations. Ancillary data in the bit stream is recovered and output serially. When the compressed audio data is at the actual bit rate, a pulse-width-modulated error signal is generated if the PCM output clock is not at the required frequency.

The decoded sampling rate, stereo mode, error status, and de-emphasis information is available in the serial status register synchronously with the beginning of the associated PCM data frame. The complete MPEG frame header can also be read from the chip.

In systems where audio/video synchronization is required, the TMS320AV120 accepts the system SCR and the audio PTS information and synchronizes the audio output to these time stamps.

PRODUCT PREVIEW

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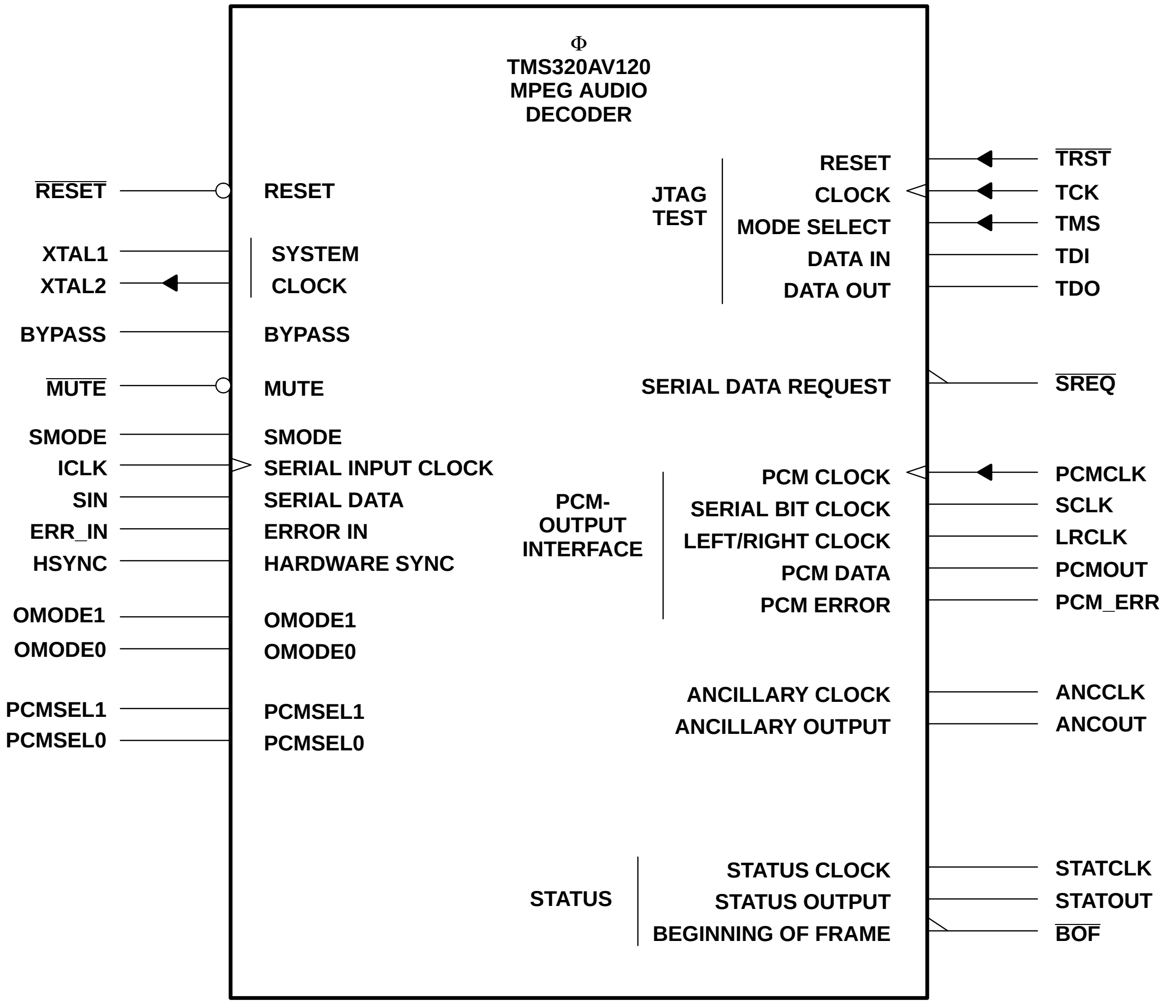
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1994.

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANCCLK	36	O	Ancillary data output clock. The rising edge of ANCCLK signals that new valid data is available on ANCOUT and can be used to latch the new data.
ANCOUT	37	O	Ancillary data output. Ancillary data from the audio frames is output serially on this terminal (see ANCCLK description).
$\overline{\text{BOF}}$	22	O	Beginning of frame output, active low. Transitions low when the data on PCMOUT is the first bit of a new frame. This signal is synchronous with SCLK.
BYPASS	14	I	Audio bypass select. When high, audio data is passed unchanged from SIN to PCMOUT. Changing to or from bypass mode requires a reset.
ERR_IN	30	I	Serial data input error. A high level at ERR_IN indicates that the incoming data may not be correct. The frame containing the invalid data will be muted if necessary. If ERR_IN is not used, it should be tied low.
GND	2, 13 24, 35		Ground
HSYNC	43	I	Hardware synchronization input. When HSYNC transitions high, the next 12 bits are assumed to be an audio-frame synchronization word. Use of this terminal is optional; if not used, it should be tied low.
ICLK	41	I	Serial-data input clock. PCM data at input SIN is set up to and loaded into the ’AV120 on the rising edge of ICLK.
LRCLK	25	O	PCM left / right channel select output. When high, the left channel is being output at PCMOUT. When low, the right channel is being output. LRCLK oscillates at the audio sampling rate. LRCLK is derived from PCMCLK and the PCMSEL terminals.
$\overline{\text{MUTE}}$	44	I	Mute select, active low. Forces muted audio output.
NC	see drwg		No connect. These terminals must be left floating.
OMODE1 OMODE0	16 15	I	Output mode select. Determines whether one or both channels of an independent dual-channel stream are output (see Table 1).
PCM_ERR	38	O	PCMCLK error signal. PCM_ERR is used for synchronization of the input and output clocks, ICLK and PCMCLK, when operating at a constant bit rate. See the section on PCMCLK error signal for the detailed functionality of this output.
PCMCLK	21	I	PCM clock input. Used to generate SCLK and LRCLK. The PCMCLK frequency is selected based on the sampling frequency and the oversampling ratio using the PCMSEL terminals (see Table 2 and Table 3).
PCMOUT	26	O	PCM serial-data output. Decompressed PCM data is output most significant bit first. PCM data is latched on the rising edge of SCLK. The PCM word size is 24 for 18-bit PCM data with the first 6 bits being zeros.
PCMSEL1 PCMSEL0	20 19	I	PCM select inputs. The PCMSEL terminals select the ratio of PCMCLK to SCLK (oversampling ratio) and the number of bits per PCM word (see Table 2).
$\overline{\text{RESET}}$	6	I	Reset, active low. The ’AV120 begins a reset sequence when this signal is low.
SCLK	27	O	Serial PCM data output bit clock. SCLK oscillates at 32 times the sampling frequency for 16-bit PCM data and 48 times the sampling frequency for 18-bit PCM data. SCLK is derived from PCMCLK and the PCMSEL terminals.
SIN	40	I	Serial data input for compressed audio data, PTS, and SCR (see SMODE description).
SMODE	42	I	Audio data/timing information select. SMODE low indicates that the data being input on SIN is compressed audio. SMODE high indicates that the data being input at SIN is either a PTS (bit 33 low) or an SCR (bit 33 high).
$\overline{\text{SREQ}}$	39	O	Serial data request input, active low. Data can be input at SIN when $\overline{\text{SREQ}}$ is low. After $\overline{\text{SREQ}}$ goes high, one additional bit of data is accepted. Subsequent data is ignored. $\overline{\text{SREQ}}$ goes high if $\overline{\text{RESET}}$ goes active (low) or the input buffer is full. $\overline{\text{SREQ}}$ does not go high as long as the input data rate does not exceed 448 kbits/second.
STATCLK	31	O	Status register output clock. The rising edge of STATCLK signals that new valid data is available on STATOUT and can be used to latch the new data. The first rising edge of STATCLK in each frame coincides with the rising edge of BOF. STATCLK is synchronous with SCLK.
STATOUT	32	O	Status register output. Data from the status register is output serially on this terminal, starting with the most significant bit (see the STATCLK description and Table 4).

PRODUCT PREVIEW

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TCK	7	I	JTAG clock input. Must be tied low for normal operations.
TDI	9	I	JTAG data input
TDO	10	O	JTAG data output
TMS	8	I	JTAG mode select input
$\overline{\text{TRST}}$	11	I	JTAG reset input, active low
V_{CC}	1, 5, 12, 23, 34		5-V supply voltage
XTAL1	3	I	Crystal or oscillator input. One side of the connection to a crystal or an external clock input. Provides the system clock to the ’AV120.
XTAL2	4	O	Crystal input, low side. Second connection (low side) to a crystal should be left unconnected when an external clock is connected to XTAL1.

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architecture

The functional block diagram of the TMS320AV120 is shown in Figure 1. The ’AV120 is a combination of a hardwired, dedicated, high-speed arithmetic unit and a micro-coded input processor. The interfaces are discussed in the following sections.

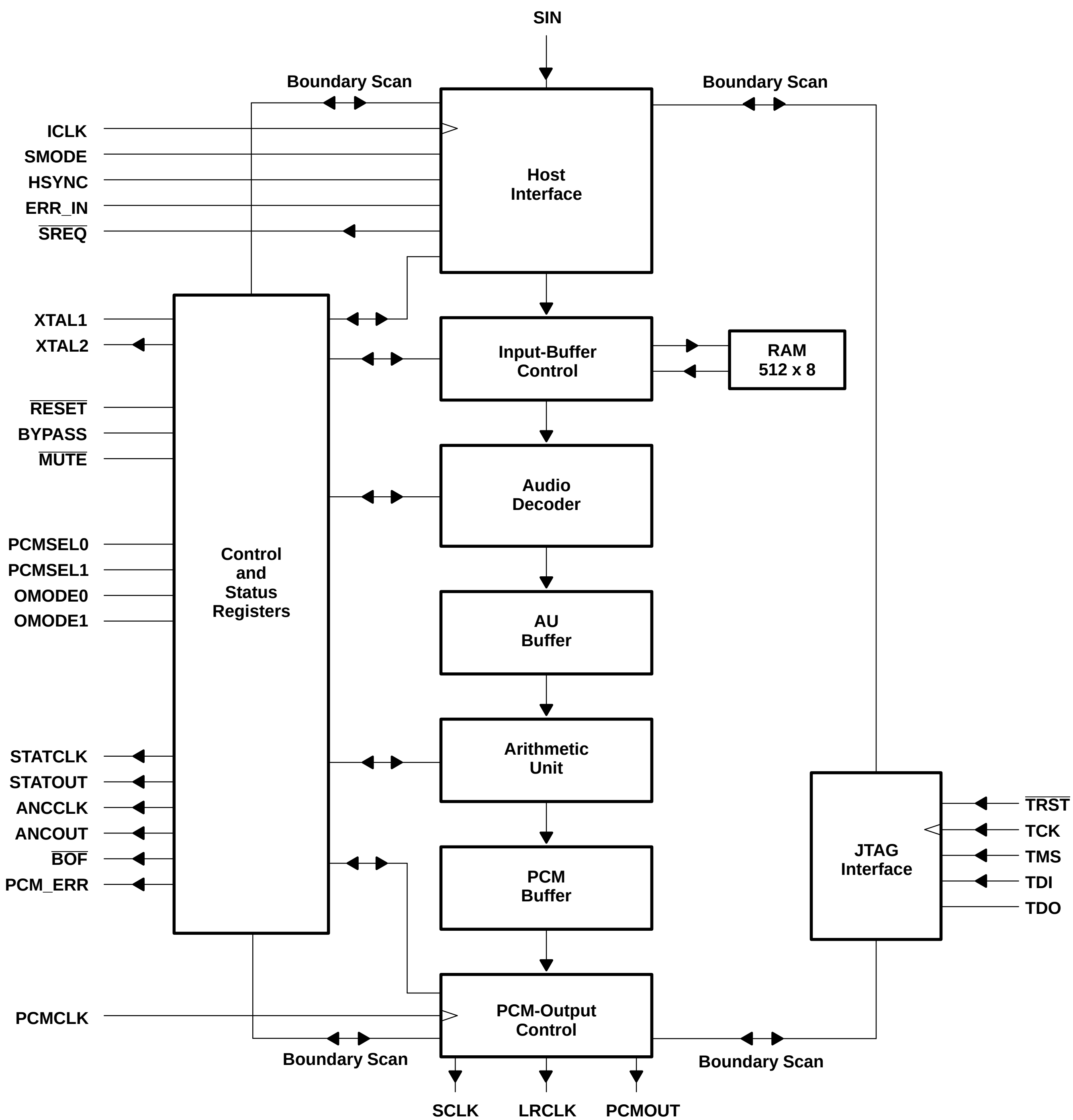


Figure 1. Functional Block Diagram

input interface

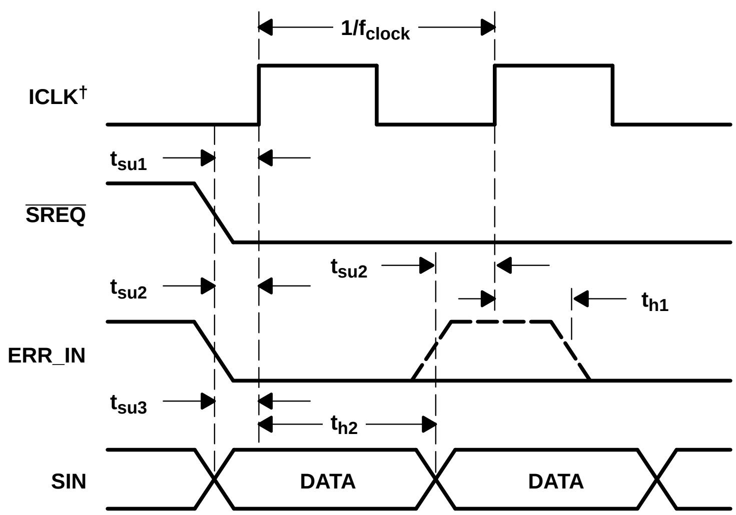
The TMS320AV120 accepts MPEG audio streams; MPEG system and packet streams cannot be decoded. Compressed data and synchronization information is input serially on SIN, using ICLK, $\overline{\text{SREQ}}$, and SMODE. Data set up on SIN is latched on the rising edge of ICLK if $\overline{\text{SREQ}}$ is low. The device accepts one additional bit of data after $\overline{\text{SREQ}}$ goes high. Data input thereafter may corrupt the bit received previously. $\overline{\text{SREQ}}$ goes high if $\overline{\text{RESET}}$ goes active (low) or the input buffer is full. A 512-byte internal buffer is used to buffer the compressed data to absorb minor input bit-rate variations. $\overline{\text{SREQ}}$ will not go high (inactive) as long as the input data rate does not exceed 448 kbits/second. Figure 2 and Figure 3 show constant-bit-rate and burst input timing.

ERR_IN is an input used to signal to the decoder that the data coming in may not be correct. The frame containing the data bit(s) that may be invalid (corresponding to ERR_IN high) will be muted if the data is from the beginning of the frame through the scale factors. The ’AV120 is capable of responding to at least one error per every 512 bytes of compressed data. This could prevent errors in the data stream from damaging speakers. If not used, ERR_IN should be tied low. Figure 2 shows the proper timing for the ERR_IN signal.

The SMODE input signals the presence of timing information. When SMODE is low, the data on the SIN terminal is interpreted as compressed audio data. When SMODE transitions high, the next 34 bits of the serial data is interpreted as either a PTS if bit 33 is a zero or an SCR if bit 33 is a one. Bit 33 should be on SIN during the same ICLK cycle that SMODE transitions high. SMODE input timing is shown in Figure 3.

An additional input, HSYNC, can be used in systems where hardware frame synchronization is available, such as the proposed EUREKA DAB systems. When HSYNC transitions high, the next 12 bits are assumed to be an audio-frame-synchronization word. If not used, HSYNC should be tied low. HSYNC input timing is shown in Figure 4.

The ’AV120 has an audio-bypass feature that allows 16-bit PCM data to be loaded into the device and passed through to the PCMDATA output. To use the audio-bypass feature, BYPASS must be set high. Changing to or from bypass mode requires a reset.



† ICLK must be at the encoded stream bit rate.

Figure 2. Constant-Bit-Rate Input Timing

input interface (continued)

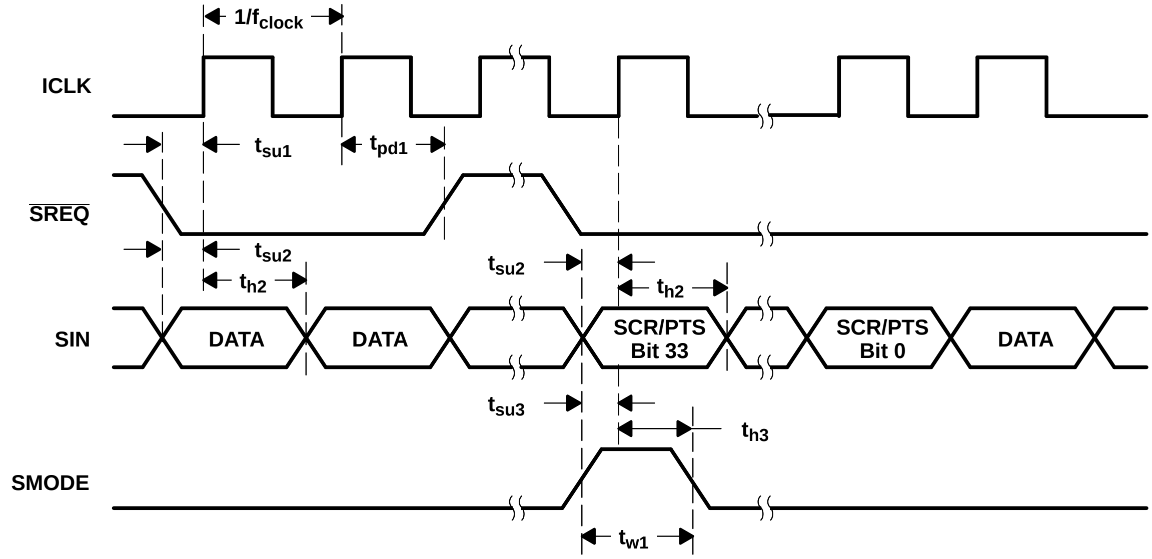


Figure 3. Burst-Data Input Timing

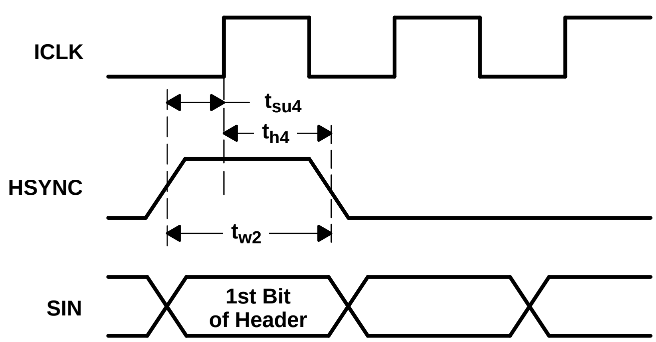


Figure 4. HSYNC Input Timing

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reset sequence

The ’AV120 must be reset on power up. Reset of the device is initiated by pulling $\overline{\text{RESET}}$ low. The following actions occur:

– $\overline{\text{SREQ}}$ goes high.
– Serial input data is ignored.
– All data buffers (including the input buffer) are cleared.
– The PCM output is forced to mute.

When the reset sequence is finished (after multiple clock cycles), $\overline{\text{SREQ}}$ again goes low signaling that the device is ready to accept compressed data input. The first high-to-low transition on $\overline{\text{BOF}}$ signals the availability of valid decoded audio data. A change in the bit rate, sampling frequency, or layer of the encoded bit stream requires a reset. If a change in one of these parameters is detected without a reset, the ’AV120 forces a reset. Figure 5 shows reset timing.

reset sequence (continued)

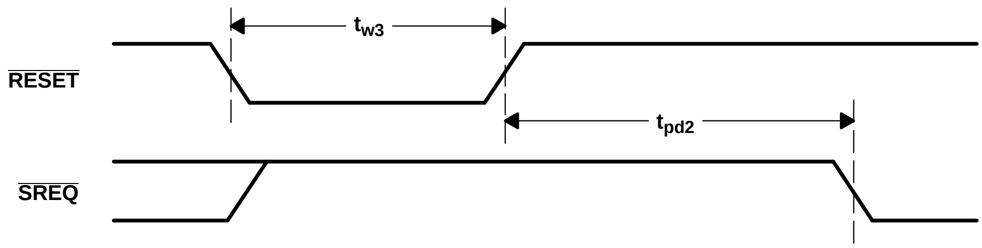

Figure 5. Reset Timing

input processor

The input processor decodes the header and prepares the audio data for the arithmetic unit. If synchronization is lost or an error is found in the header or during the CRC check (if the bit stream is protected), the PCM output for that frame is muted. The status register is updated to signal a synchronization or CRC error.

PCM output interface

The decoded audio data is output in serial PCM data format on PCMOUT. The data is output with the most significant bit first. PCM data can be latched on the rising edge of the serial PCM output clock (SCLK). The data output on PCMOUT alternates between the two channels as designated by LRCLK. If the input data stream is monophonic, the same PCM data is output on both channels. As shown in Table 1, if the input data stream is dual channel (two independent channels), the channel(s) output depends on the setting of OMODE.

Table 1. OMODE1 and OMODE0 Functional Summary

OMODE1 – 0	LEFT-CHANNEL OUTPUT	RIGHT-CHANNEL OUTPUT
00	Channel 0	Channel 1
01	Channel 0	Channel 0
10	Channel 1	Channel 1
11	Invalid	Invalid

The PCMSEL terminals select the ratio of PCMCLK to SCLK and the number of bits per PCM word. If the PCM word size is 24, the first 6 bits are zeros followed by an 18-bit PCM value. Output precision and PCM word length are selected by the PCMSEL terminals as shown in Table 2.

Table 2. PCMSEL1 and PCMSEL2 Functional Summary

PCMSEL1 – 0	PRECISION	PCMCLK	PCM WORD LENGTH
00	16 bits	1 ×	16 bits
01	16 bits	256 ×	16 bits
10	18 bits	1 ×	24 bits
11	18 bits	384 ×	24 bits

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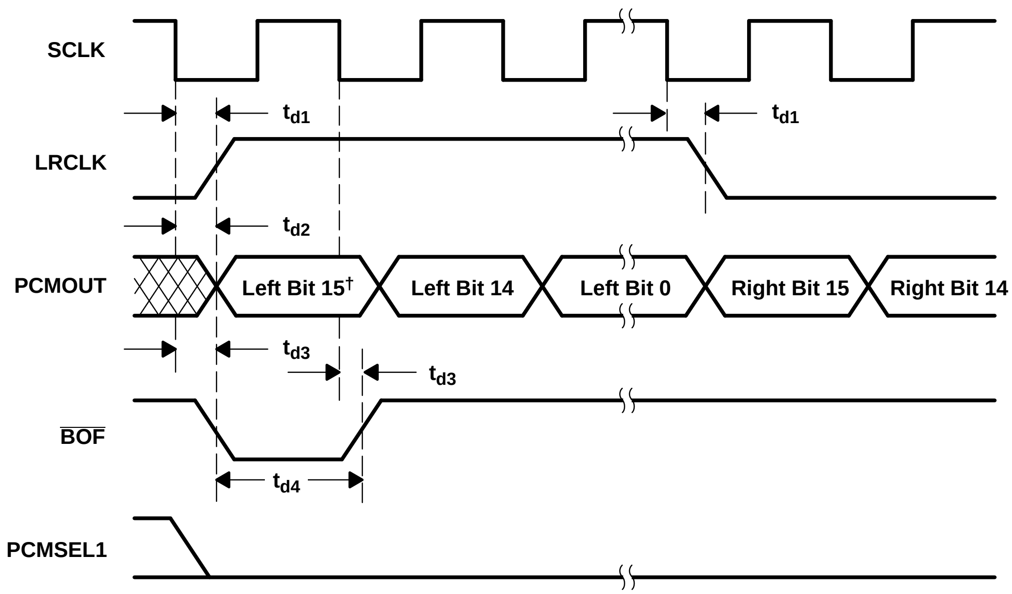
PCM output interface (continued)

The decoder requires a clock input (PCMCLK) that is at the proper multiple of the sampling frequency, as indicated by the SF1:0 bits in the status register and the PCMSEL terminal. The PCMCLK input frequency depends on the sampling frequency and oversampling ratio as shown in Table 3. PCM output timing is shown in Figure 6.

Table 3. PCMCLK Frequency Selection Summary

SAMPLING FREQUENCY (kHz)	16-BIT PCM WORD LENGTH		24-BIT PCM WORD LENGTH	
	PCMCLK = 1 x SCLK (MHz)	PCMCLK = 256 x SCLK (MHz)	PCMCLK = 1 x SCLK (MHz)	PCMCLK = 384 x SCLK (MHz)
32	1.024	8.192	1.536	12.288
44.1	1.4112	11.2896	2.1168	16.9344
48	1.536	12.288	2.304	18.432



† First bit of frame as indicated by $\overline{BOF}$

Figure 6. PCM Output Timing

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ancillary-data-output interface

Ancillary data from each frame is output serially on ANCOUT. The rising edge of ANCCLK signals new valid data is available on ANCOUT and can be used to latch it. When ANCCLK is switching, its frequency is equal to one-half of the system clock at the XTAL1 input. If ancillary data is not needed for a specific application, these terminals can be ignored. Figure 7 shows ancillary-data-output timing.

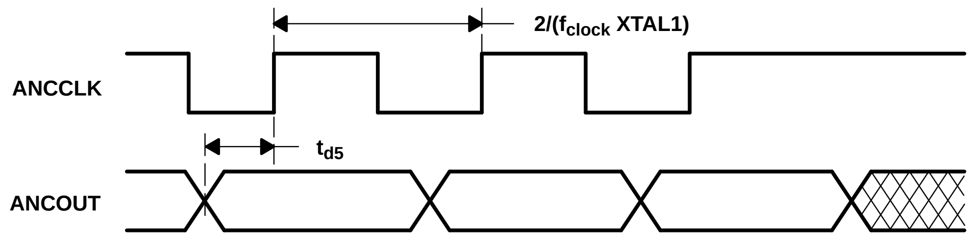

Figure 7. Ancillary-Data-Output Timing

status-register-output interface

The status register contains information from the header of each frame and on the status of the device. The register can be read serially on STATOUT starting with the most significant bit (see Figure 8). Data is valid on the rising edge of the STATCLK output. When STATCLK is switching, its frequency is equal to SCLK. The status register is updated on the high-to-low transition of the $\overline{\text{BOF}}$ signal. Table 4 shows the status-register-output order. Stereo mode, sampling frequency, and de-emphasis information is output at the begining of the status-register stream for convenience in addition to the MPEG header.

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status-register-output interface (continued)

Table 4. Status-Register-Output Order

BIT LOCATION	DESCRIPTION	FUNCTION
32	Stereo mode	1 = Dual mono 0 = All others
31:30	Sampling frequency	00 = 44.1 kHz 01 = 48 kHz 10 = 32 kHz 11 = Reserved
29:28	De-emphasis mode	00 = None 01 = 50/15 microseconds 10 = Reserved 11 = CCITT J.17
27	SYNC status	1 = Chip is in SYNC-recovery mode 0 = Locked
26	CRC status	1 = CRC error found 0 = No error or CRC not enabled in the encoded bit stream
25	PCM underflow	1 = PCM-output underflow 0 = Normal operation (no underflow)
24	MPEG-frame header without sync word	ID
23:22		Layer
21		Protection bit
20:17		Bitrate index
16:15		Sampling frequency
14		Padding bit
13		Private bit
12		Mode
11:10		Mode extension
9:8		Copyright
7		Original/home
6:5		Emphasis
4:1	Version number	’AV120 device revision ID
0	Reserved	

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status-register-output interface (continued)

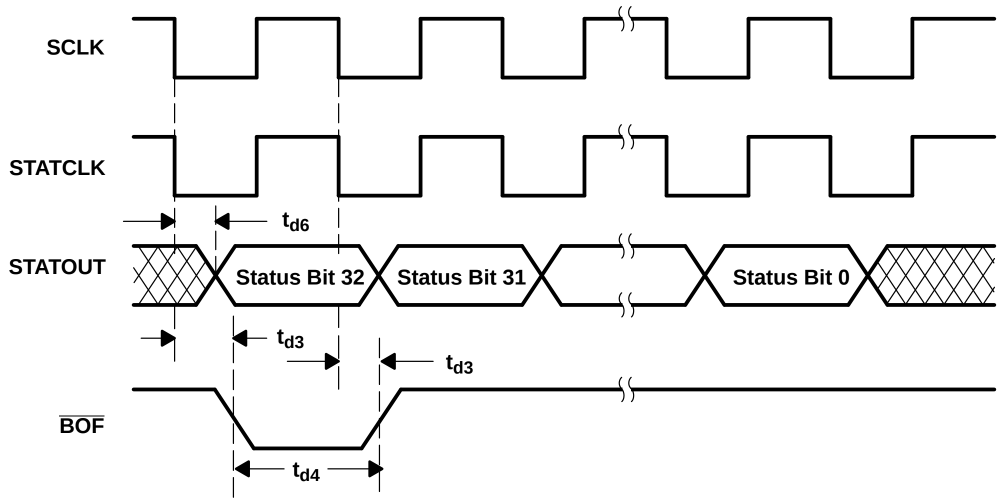

Figure 8. Status-Register-Output Timing

audio/video synchronization

In systems where audio/video synchronization is required, the TMS320AV120 has the capability of interpreting and comparing the system clock reference (SCR) and the audio presentation time stamp (PTS). Since both the SCR and the PTS are present only at the pack and packet level of the MPEG bit stream, and not in the audio frames, they have to be supplied to the TMS320AV120 from the system controller.

The SCR and PTS information is transmitted to the TMS320AV120 over SIN, MSB first, multiplexed with the compressed audio data. The SMODE input signals the presence of timing information. When SMODE is low, the data on SIN is interpreted as compressed audio data. When SMODE transitions high, the next 34 bits of the serial data is interpreted as either a PTS if bit 33 is a zero or an SCR if bit 33 is a one.

The system is expected to transmit all PTS stamps to the TMS320AV120 as found in the system stream. SCR information (updated at the 90-kHz rate) should be transmitted to the audio decoder about once a millisecond.

The TMS320AV120 compares the PTS associated with the frame being output with the latest SCR. When the delta reaches the duration of one frame, the ’AV120 either delays or attempts to catch up until the times match. While the chip can always delay, it can only catch up if the compressed data input is at a rate higher than the actual bit rate. During both delay and catch-up operations, PCMOUT is muted. If synchronization is required, the data should be available to the TMS320AV120 when requested by the SREQ control signal. For designs that do not need synchronization, tie SMODE low.

PCMCLK error signal

In order to facilitate synchronization of the PCMCLK frequency to the input data rate, the TMS320AV120 generates an error signal that is proportional to the average difference between the ICLK and the PCMCLK frequencies. The error signal is a pulse-width-modulated pulse train at a frequency equal to twice the sampling frequency. A 50% duty cycle indicates no error (see Figure 9). A VXO control voltage is derived from the PWM signal by low-pass filtering and any required level shifting. The adjustment range is planned to be in the ±0.1% range, with an integration time of approximately 2 seconds giving a very stable, low-loop-gain system.

The PCM_ERR signal is only valid when the compressed data input is at a rate at or below 448 kbits per second. In general, the SREQ signal must be low at all times for the error signal to be valid. This is the exact opposite of the input data rate required for audio/video synchronization — the two modes cannot be used at the same time.

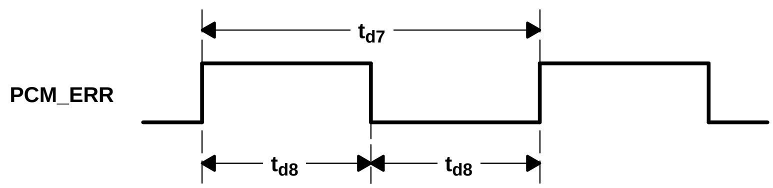

Figure 9. PCM_ERR-Output Timing

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.5 V to 6 V
Input voltage range, V_I . . . . –0.5 V to (V_{CC} + 0.5 V)
Output voltage range, V_O . . . . –0.5 V to (V_{CC} + 0.5 V)
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±20 mA
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage		–0.5		0.8	V
I_{OH}	High-level output current					mA
I_{OL}	Low-level ouput current					mA
f_{clock}	Clock frequency	System clock (XTAL1)	22		26	MHz
		PCMCLK			20	MHz
		ICLK constant bit rate			448	kHz
		ICLK burst			10	MHz
dt/dV	Input transition (rise or fall)		0		10	ns/V
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = –8 mA	3.7			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	I_{OL} = 8 mA			0.5	V
I_I	Input current	V_{CC} = 5.25 V,	V_I = V_{CC} or 0 V			±1	µA
I_{OZ}	Off-state output current	V_{CC} = 5.25 V,	V_O = V_{CC} or 0 V			±5	µA
I_O	Output current, TDI and TMS	V_O = 0 V			–325		µA
		V_O = V_{CC} – 1.5 V			–150		
I_{CC1}	Supply current, operating	V_{CC} = 5.25 V					mA
I_{CC2}	Supply current, quiescent	V_{CC} = 5.25 V,	V_I = V_{IH} or V_{IL}				mA
C_i	Input capacitance§	f = 1 MHz			8		pF
C_o	Output capacitance§	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the capacitance at an input, output, or I/O terminal.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

pulse durations

		FIGURE	MIN	MAX	UNIT
t_{w1}	SMODE high	3	100		ns
t_{w2}	HSYNC high	4	100		ns
t_{w3}	$\overline{\text{RESET}}$ low	5	200		ns

setup times

		FIGURE	MIN	MAX	UNIT
t_{su1}	$\overline{\text{SREQ}}$ output low before ICLK↑	2, 3	25		ns
t_{su2}	SIN before ICLK↑	2, 3	25		ns
t_{su3}	SMODE high before ICLK↑	3	25		ns
t_{su4}	HSYNC high before ICLK↑	4	25		ns

hold times

		FIGURE	MIN	MAX	UNIT
t_{h1}	ERR_IN after ICLK↑	2	5		ns
t_{h2}	SIN after ICLK↑	2, 3	5		ns
t_{h3}	SMODE after ICLK↑	3	5		ns
t_{h4}	HSYNC after ICLK↑	4	5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

propagation delay times

		FIGURE	MIN	MAX	UNIT
t_{pd1}	ICLK↑ to $\overline{\text{SREQ}}$ high	3		250	ns
t_{pd2}	$\overline{\text{RESET}}$ high to $\overline{\text{SREQ}}$ low	5			ns

delay time relationships

		FIGURE	MIN	MAX	UNIT
t_{d1}	LRCLK after SCLK↓	6		50	ns
t_{d2}	PCMOUT after SCLK↓	6		50	ns
t_{d3}	$\overline{\text{BOF}}$ after SCLK↓	6, 8		50	ns
t_{d4}	$\overline{\text{BOF}}$↓ to $\overline{\text{BOF}}$↑ (pulse)	6, 8	400†		ns
t_{d5}	ANCOUT before ANCCLK↑	7	25		ns
t_{d6}	STATOUT after STATCLK↑	8	50		ns
t_{d7}	PCM_ERR output period	9		163.8	µs
t_{d8}	PCM_ERR output pulse width, high or low	9	.04	163.8	µs

† $\overline{\text{BOF}}$ pulse is approximately 1 SCLK period in duration.

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