Fuzzy Logic-Based Internal and External SOC Meters for Li/SO_2 Cells

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Abstract

Since 1997, Villanova University and US Nanocorp, Inc. have been developing fuzzy logic-enabled hardware for the measurement of the state-of-charge (SOC) of primary Li/SO_2 cells. This hardware has been based on two approaches – coulomb counting and impedance. These approaches are suitable for internal and external SOC meters, respectively. The design of a dedicated integrated circuit chip based on coulomb counting and a preliminary design of an impedance-based meter have been previously reported [1]. A dedicated hardware chip has been designed and implemented in a field programmable gate array (FPGA) chip. More details on the design of this chip and test results on Li/SO_2 cells will be presented in this paper. Until now, we have only provided limited details of the design of the impedance meter circuitry. Here we provide design and implementation details on the impedance-based meter.

Introduction

Primary lithium sulfur dioxide (Li/SO_2) batteries are used in the Army's SINCGARS communications radio. A major difficulty in determining the state-of-charge (SOC) of Li primary batteries is their flat discharge profiles. Two approaches have previously been used to determine the SOC of primary Li/SO_2 batteries.

The first method used by Atwater [2] is a coulomb counting approach. In this approach the charge flowing out of the battery is accumulated until one coulomb of charge has been collected. This amount is adjusted for battery temperature and discharge rate using an empirically-derived "discharge efficiency". This adjusted charge is then subtracted from the battery's nominal capacity for the first calculation, or from the previous SOC determination for subsequent calculations. The discharge efficiency data is stored in lookup tables and the hardware is relatively low cost for this type of sensor. This approach works well when the operating conditions match the empirical data points. However, the interpolation capability for conditions lying between empirically-derived data points is not necessarily good with this approach. We have previously reported fuzzy logic approaches that provide a more efficient means of determining cell SOC using this Coulomb counting data [3,4].

A second approach developed by Peled [5] provides an external means of determining the SOC of primary Li/SO_2 batteries. In this approach, the voltage recovery profile of the battery is measured following a pulsed discharge. The temporal profile of the recovery of the battery voltage is used to determine the SOC of the battery. This approach works under certain conditions but is not always reliable.

SOC Meters for Primary Li/SO_2 Cells

Coulomb Counting-based SOC Meters

We have developed two approaches to determining the SOC of primary Li/SO_2 cells – one suitable for an *internal* meter based on coulomb counting and another suitable for an *external* meter based on cell impedance measurements. In both cases the methodology used to determine the SOC of the batteries is a fuzzy logic one.

The internal meter is based on coulomb counting which integrates current over time. Since battery capacity is dependent on both the discharge rate and the temperature of the cell, compensation for these factors is required in order to provide accurate SOC determination. Initially, we used the data measured by Atwater [2] (summarized in Fig. 1), showing battery capacity dependence on rate and temperature, as the basis for compensating available battery capacity in our coulomb counting-based meter designs.

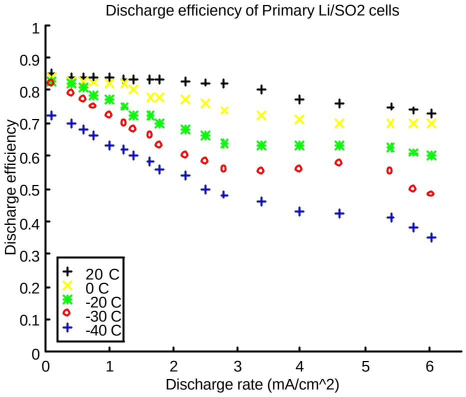

Fig. 1. Discharge efficiency curves for Li/SO_2 cells.

A fuzzy logic model of this system was developed (see refs. [3, 4] for details) which took as inputs the cell temperature and the discharge current and output the discharge efficiency.

This was then used to compensate for the available capacity of the battery. The cell SOC was initially set at 100%. As the battery was being discharged, the available capacity was calculated by integrating the discharge current, subtracting this from the previously determined capacity and dynamically adjusting the available capacity using the discharge efficiency calculated by the fuzzy logic model. The advantage of this approach compared to using a lookup table in this case is that the fuzzy logic model is very code efficient (occupying only about 300 bytes of memory). Additionally, the fuzzy logic model allows for accurate, nonlinear interpolation between measured data points, a difficult task to accomplish analytically in a code efficient manner. Finally, this approach can also be extended to compensate for other factors in a secondary battery (such as cycle number, self-discharge, battery aging, *etc.*) which would not be easily implemented in lookup tables.

The coulomb counting meter, including the fuzzy logic algorithm, has been implemented in hardware using both a Motorola 68HC11 microcontroller and a Motorola 68HC12 microcontroller (see ref. [1] for details). We have also designed an application specific integrated circuit (ASIC) digital fuzzy processor/coulomb counting chip which may be integrated directly into a battery. This chip was designed to 1) take digital current and temperature inputs and calculate, by a fuzzy system approach, the discharge efficiency of the Li/SO_2 cell and 2) perform charge accumulation. As output, the chip provides two 4-bit outputs which provide a decimal count decrement from 99 to 0 representing the percentage of nominal battery capacity available. This decrementing of the SOC is adaptively modified with changing temperature and discharge rate conditions every time 1C of charge has been extracted from the battery.

The gate level design of this chip was performed in the VHDL hardware description language using Mentor Graphics engineering design automation (EDA) tools. Details of the design are given in ref. 1. Field programmable gate arrays (FPGAs) provide a low-cost, gate-level design verification step prior to the detailed transistor-level design stage. This low cost verification step is important to perform prior to full ASIC design and chip fabrication because of the relatively high cost associated with this latter stage of IC development. A Lucent Technologies OR2c40A 40,000 gate FPGA chip was used to verify our design at the gate level. Different combinations of current and temperature were fed in a digital form to the input pins of the chip and the output pins were tied to LCD display elements on an ORCA development board containing the OR2c40A chip. The LCD display elements were observed to change both in the manner expected and at the times expected for different combinations of input current and temperature as a discharging Li/SO_2 cell was being monitored by the FPGA chip.

Having verified the gate level design in the FPGA implementation, a full transistor-level ASIC design was performed. Again the Mentor Graphics EDA design tools were used to perform the transistor level layout. The process targeted for the design was a 2.0 μm minimum feature size, n-well process. Rather than performing a full custom design, a standard cell, semi-custom design approach was adopted. The standard cell libraries used were from the Mentor Design Kit (MDK) set from Mentor Graphics. However, the pad frames available from the Mentor Graphics set were too small to accommodate our design and so individual pads were downloaded from the MOSIS web site and manually incorporated into the chip layout. The IC design without the pad frame was simulated and found to both perform correctly and not violate any process design rules. On the other hand, simulation of the pads resulted in several errors which were apparently not real errors but were associated with errors in the way that the pads were read by the Mentor Graphics tools. When the pads were simulated in another EDA software package, MAGIC, no errors were found. The design was submitted to MOSIS for fabrication. However, when the manufactured chips were tested, a short between the power supply input and ground pins was observed. In reviewing the design again, an error in translation was found between the pad layout in MAGIC and the layout in the Mentor Graphics tools. The pad layout in MAGIC displayed two lines entering the pad whereas in the Mentor Graphics tool, only one line was seen to enter the pad. We believe that the shorting was a result of incorrectly wiring the pad power supply/ground connections. We will rework the pad layout designs and resubmit the design in the future, since we believe (based on our circuit simulations of the core design) that the rest of the design works correctly.

Impedance-Based SOC Meter

In addition to the coulomb counting approach, which is suitable for an internal meter, an impedance-based meter (suitable for use as an external meter) has also been designed and its implementation is close to completion. While a general description of the design of this meter has been presented previously [1,7], we present here a more detailed description.

A detailed system level block diagram is shown in Fig. 2. Three ac sources provide sinusoidal voltage signals (of approximately 10 mV amplitude) at three frequencies – 10Hz, 40 Hz and 1 kHz to the Li/SO_2 cell. There are two modes of operation of the circuit – a discharge mode and a measurement mode. In the discharge mode, the cell is discharged through an electronic load. We have found it necessary to discharge the Li/SO_2 cells at a high discharge rate (approx. 200 mA for 1/3"C"-size cells) to sufficiently remove the passivation layer (that forms over time on the Li anode) so as to obtain reliable and reproducible impedance measurements. The switch control circuit temporarily connects the Li/SO_2 cell under test to an electronic load (for 30 sec) to invoke this pre-discharge step after which the cell is automatically connected to the measurement circuit. The tracking DC source provides an offset DC voltage equal to the closed circuit voltage of the cell under test to prevent any DC voltage being fed into the lock-in amplifier (phase detector circuit). The lock-in amplifier (phase detector) circuit is used to provide good signal-to-noise ratio in the measurement. Since the amplitude of the applied ac signal is very small (approx. 10mV) a noise averaging technique, such as phase sensitive detection, is required to produce measurements with acceptable signal-to-noise ratio. The individual circuits are now described in more detail.

The ac sources have been implemented using a Wien bridge oscillator topology built around the LM358 op amp. The measurement amplifiers (amplifiers 1 and 2 in Fig. 2) are identical and comprise a matched pair of LM358 op amps feeding into a LM741 op amp (see Fig. 3). The resistors R_2, R_3, R_4, and R_5 must be within a 1% tolerance to ensure high accuracy. The two capacitors C_1 and C_2 and the resistor R_6 make up a high pass filter, ensuring that V_0 is an ac signal.

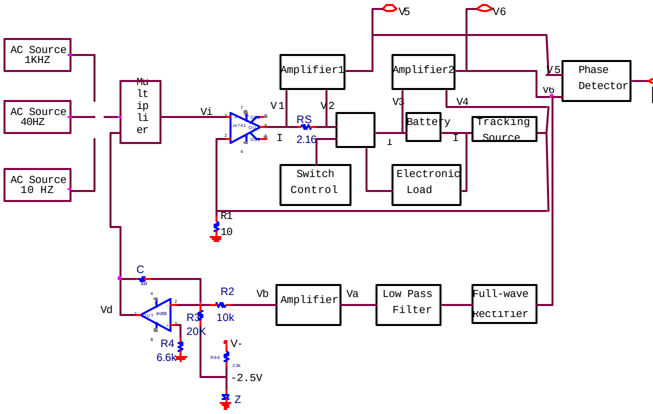

Fig. 2. Detailed System Level Block Diagram

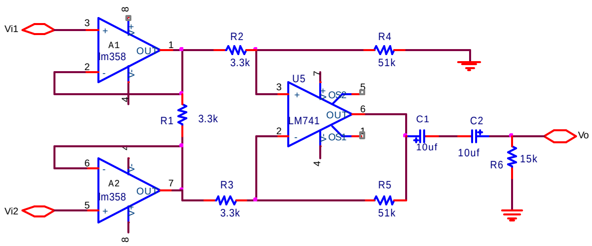

Fig. 3. Measurement amplifier circuit

A relay is used to switch the circuit between the discharge mode and the measurement mode. A transistor driver operated in a switching mode is used to turn on and off the relay. The 30 sec timing of the discharge mode is set by the discharge of a resistor through a capacitor. The circuit for the switch control circuit is shown in Fig. 4.

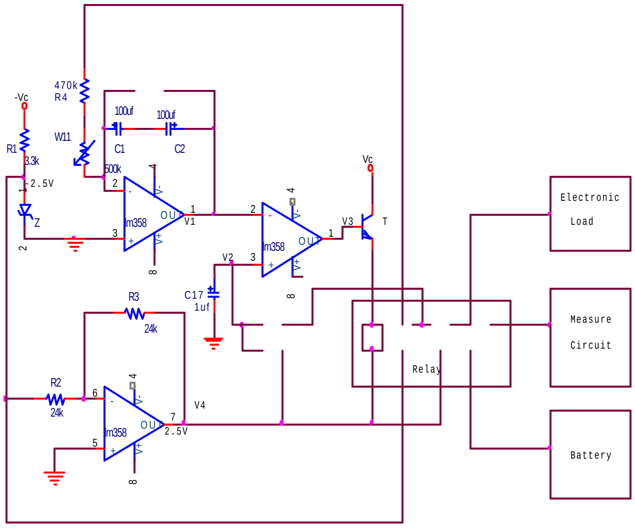

Fig. 4. Switch control circuit.

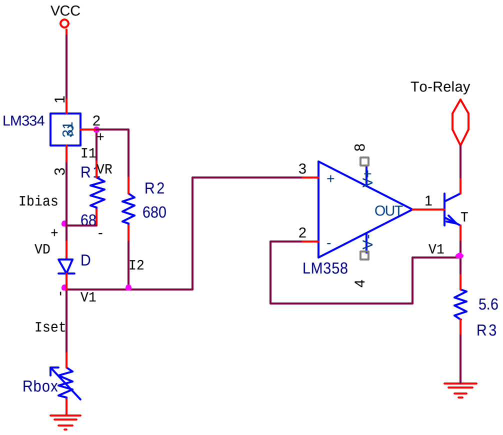

Fig. 5. Electronic Load Circuit

The electronic load uses an LM334 current source as the load with a diode to provide temperature compensation for this device. The discharge current can be set using a potentiometer. The electronic load circuit is shown in Fig. 5.The tracking DC source circuit should track the DC voltage of the battery under test since the cell voltage will drop as the battery discharges. The circuit design is shown in Fig. 6 and consists of four stages – input and output buffer stages, and two negative feedback amplifiers. By using two amplifiers, the phase of the output is ensured to be the same as the phase of the input. The two 33 μF capacitors are used to filter out the AC component of the signal ensuring that only DC voltage is output. The output transistor provides a constant 15-20 mA current through resistor R_5 to ensure correct functioning of the circuit.

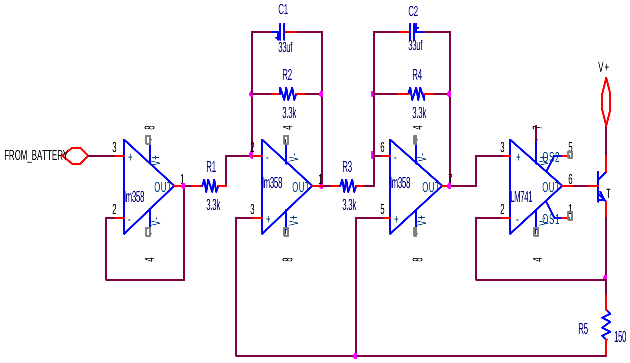

Fig. 6. Tracking DC source Circuit

The phase sensitive detector circuit is shown in Fig. 7. There are several stages to this design. The input scaling preamplifiers A_1 and A_2 feed into two comparator circuits which convert the sinusoidal signals to square wave signals. The third stage of the phase sensitive detector circuit is an active half-wave rectifier which inverts and half-wave rectifies the signals. The zener diodes, Z_1 and Z_2 are used to ensure that the amplitudes of the two signals being fed into the third stage are identical. The fourth stage of the phase detector circuit is a difference amplifier, such that the output voltage $V_e = V_c - V_d$. This difference voltage is directly proportional to the phase difference between the two input signals to the phase detector circuit. The remaining circuits are a second half-wave rectifier followed by a 4th order low pass filter. These circuits produce a DC output which is directly proportional to the phase difference between the two input signals.

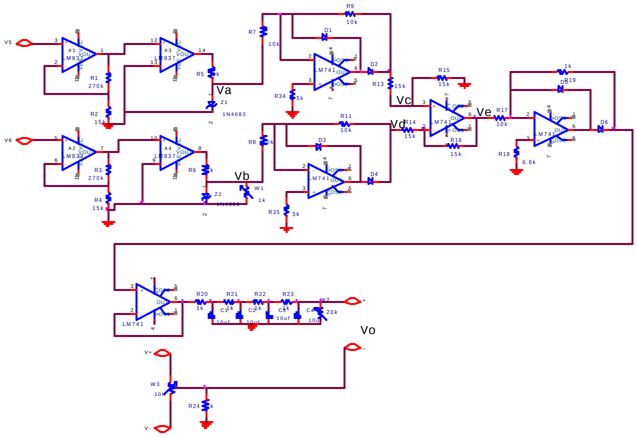

Fig. 7. Phase Sensitive Detector Circuit

Finally, a precision full-wave rectifier designed around the LM358 op amp, another 4th order low pass filter network, and an output amplifier circuit were designed and implemented. These circuits are shown together in Fig. 8. The entire circuit was breadboarded and tested on 1/3"C"-size Li/SO_2 cells and found to give results similar to those obtained from a Solartron 1250 Frequency Response Analyzer driven by a PAR273 potentiostat/galvanostat. The circuits were then laid out using Orcad printed circuit board (PCB) layout tools as two distinct boards – one containing the phase sensitive detector circuitry and the other containing the remaining circuitry. The boards have been populated with components and are currently undergoing final debugging and calibration. The final stage of development of the impedance meter is the interfacing of the impedance measuring unit (the circuitry described above) to a microcontroller. The microcontroller is used to 1) acquire the phase and amplitude of the Li/SO_2 cell, 2) calculate the Li/SO_2 cell's SOC from the cell's impedance amplitude and phase (at the three frequencies specified earlier) using a stored fuzzy logic-based algorithm, and 3) output the result to a liquid crystal display. Progress towards this final goal will be described at this conference.

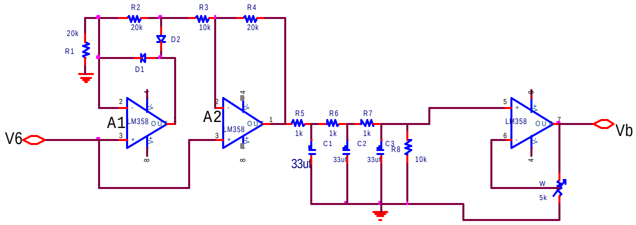

Fig. 8. Precision Full-Wave Rectifier, Low Pass Filter and Output Amplifier Circuits

Conclusions

In this paper we have described several approaches to the design and fabrication of fuzzy logic-based SOC hardware for Li/SO_2 cells. We have successfully implemented internal meters using two different microcontrollers and FPGAs. Although an ASIC chip has also been designed, layout errors associated with the pad frame and not the core design has delayed acquisition of a fully functional chip. We have also presented a detailed description of the design of fuzzy logic-based impedance hardware that can be used to work as an external meter for Li/SO_2 cells.

Acknowledgments

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