

Fuzzy Logic-Based Smart Battery State-of-Charge (SOC) Monitor for SLI Batteries

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Abstract

Automotive starting, lighting, and ignition (SLI) lead acid batteries are prone to capacity loss due to low temperature, self-discharge, sulfation, and shorting of plates. Monitoring and charge control of these batteries can be improved by using the concept of a smart battery system (SBS). In the present work, a smart battery monitor has been designed and manufactured. This monitor utilizes patented fuzzy logic-based methods [1]. Data for battery temperature, voltage and current are acquired for accumulation through the coulomb counting method and the fuzzy logic model of the system is used to determine the battery's SOC, compensating for temperature and discharge rate. This specially-designed and fuzzy logic model-based monitor has been implemented in 0.5 μm CMOS technology. The gate level and transistor level simulations have been successfully completed and now the custom chip is being tested. The main functions and test results of this fabricated smart battery SOC monitor integrated circuit (IC) chip are presented.

Introduction

Monitoring SOC is crucial for improving the life and performance of SLI lead acid batteries. Since 1997, Villanova University and US Nanocorp, Inc. have collaborated on the development of patented fuzzy logic-based methods for determining SOC and state-of-health (SOH) of a battery [1,2]. In order to implement the fuzzy logic algorithm for battery SOC determination, many special calculations are required and memory space is required to store both the fuzzy logic model itself and the results of intermediate calculations. Commercial microprocessors usually cannot implement the fuzzy logic algorithm efficiently and so we are developing our own SOC monitor chip to efficiently perform fuzzy logic calculations. This SOC monitor chip is part of a smart battery controller which will be embedded in an automotive battery (producing a 'smart battery') and will include a

communications interface so that the smart automotive battery can report its SOC to a central computer on the vehicle.

The battery temperature, voltage and current are required inputs for the fuzzy logic model to accurately compute the battery SOC. A four-channel A/D converter has been designed for this monitor so that these analog signals can be converted to digital signals and then fed to the digital controller of the SOC monitor chip. The SOC monitor chip is a mixed signal IC design incorporating both analog and digital circuitry. The digital part is designed using a hardware description language (VHDL) after which the VHDL design is converted to an IC layout. The analog circuitry is laid out manually. After both the analog and digital circuits layouts are completed successfully, they are combined and the entire circuit simulated prior to submitting the complete IC design for manufacture. In this paper, we present the design of the chip and recent results obtained for a fuzzy logic-based SOC monitor chip fabricated in 0.5 μm CMOS technology.

Principle and Architecture of SOC Monitor Chip

In a SBS, sensors for acquiring battery data are embedded in the battery package, and then these sensors send the acquired data to a smart battery controller. The smart battery SOC monitor uses coulomb counting to accumulate the battery current and uses the fuzzy logic model of the battery to determine its SOC, compensating for temperature and discharge rate. Coulomb counting is a current integration process as described mathematically by Eq. 1. The fuzzy logic algorithm to compensate for SOC variation with temperature and discharge rate is developed using the methods described in ref. [1].

$$Q = \int_0^T I(t)dt = \sum_{i=0}^n I(t_i) \cdot \Delta t \quad (1)$$

where $\Delta t = T/n$, $t_i = i \cdot \Delta t$.

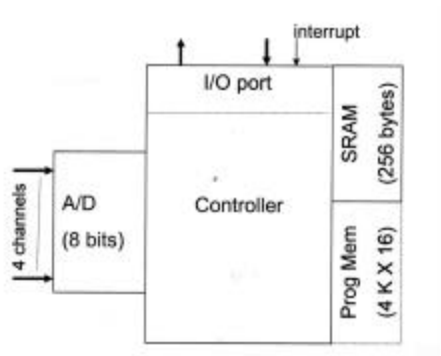


Figure 1 Architecture of SOC Monitor

The architecture of the SOC monitor is shown in Fig. 1. The controller chip comprises:

- two 8-bit parallel ports
- one interrupt source
- 12-bit program address bus
- 16-bit program data bus
- 12-bit common address bus
- 8-bit common data bus
- Arithmetic logic unit

The instruction set for the digital controller includes the basic control commands (e.g., move, jump, etc.) and three special instructions for implementing the fuzzy logic algorithm: *fuzzify*, *infer*, and *defuzzify*. While the fuzzy logic approach offers high code efficiency, allowing for on-chip FLASH memory to be used to store the fuzzy logic algorithm, in the present implementation, external program memory (4k x 16) is being employed. Additionally, on-chip SRAM will also be incorporated into the chip for intermediate data storage but an external SRAM chip (256 bytes) is being used in the present prototype. In order to access the external analog signals, a 4-channel A/D converter is integrated with this monitor. The designed IC chip and its bonding diagram are shown in Fig. 2.

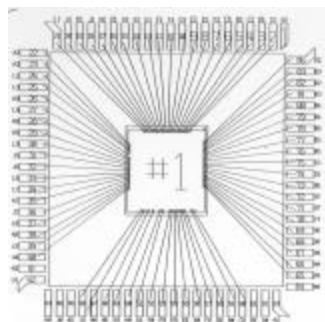


Figure 2 SOC Monitor Chip and its bonding diagram

Fuzzify, Infer and Defuzzify are three fuzzy logic commands [3,4,5]. Because of their inclusion, battery SOC can be calculated quickly and efficiently. The flow chart for these three commands is shown in Fig. 3. From Fig. 3, it can be seen that the fuzzification of the input variables, the rules processing (Infer) of the fuzzified data, and the defuzzification of the inferred data are continuous and efficient. Without these specialized fuzzy commands, the fuzzy logic calculations would be at least 10X slower. Additionally, extra program memory would need to be included to perform the fuzzy logic calculations. Therefore, inclusion of the fuzzy logic commands, both increases the speed of the fuzzy logic algorithm and reduces the program memory size.

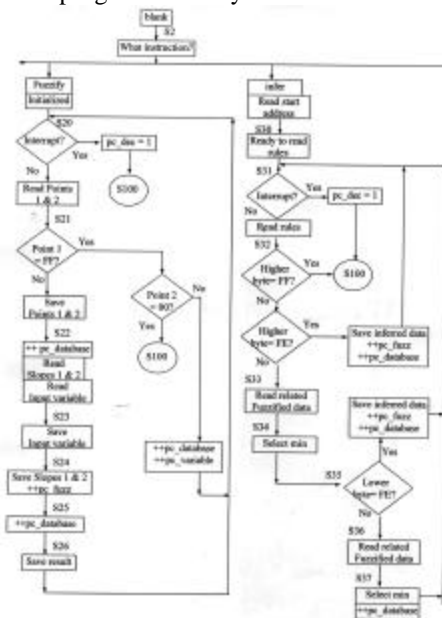


Figure 3.1 Flowchart for Fuzzify and Infer Commands

The program memory of our SOC monitor design is limited to $4k \times 16$ and the program and the fuzzy logic model share this memory. Thus it is important that the memory be mapped efficiently. There should be enough space reserved for the fuzzy logic model, but reserved memory not used by the fuzzy logic model should still be available as program memory. Since the fuzzy logic model is developed prior to programming in the monitor IC, the fuzzy logic model's exact size is known in advance and the remaining program memory may then be allocated for the program. The main structure of the program memory is shown in Fig. 4. $0 \times XXX$ denotes the end address for the fuzzy logic model, and the start address for the fuzzy logic model is always fixed at $0 \times C00$.

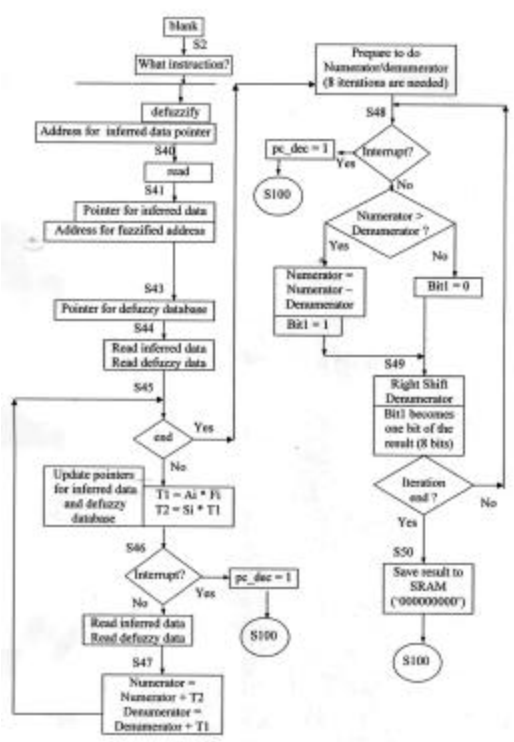


Figure 3.2 Flowchart for the Defuzzify Command

Address (12 bits)	Content (16 bits)
0x000	Start of program
0x001	program
.....
0xc00	Start address for fuzzy model database
0xc01	...
0xc02	...
.....
0cXXX	End of fuzzy model database
0cXXX+1	program
.....
0cfff	program

Figure 4 Structure of Program Memory

There are a total of 27 basic instructions and 3 fuzzy logic instructions. All of these instructions have been verified at the functional level, the gate level and the transistor level. These three levels represent three different design stages [6,7]. First the functional level simulation had to be successfully accomplished, and then the VHDL design was converted to the gate level design if the functional file was synthesizable, otherwise the VHDL file had to be modified. The

Mentor Graphics tools VSIM, VCOM and Leonardo were used for these simulations [8]. In order to ensure the correctness of the gate level design, the gate level design was also verified in a field programmable gate array (FPGA) development system. This FPGA test was completed with ORCA FPGA development system from Lucent Technologies [9]. Once the gate level simulation was successfully achieved and verified in hardware, then the gate level design was directly converted to a transistor level design and the transistor level design simulated using Accusim simulation software [8]. This transistor level was the most difficult stage. The correctness of the transistor-level circuit simulation does not mean that the design must be correct. Many process design rule checks needed to be performed. Only after all the simulations were correct and the design rule checks were passed, could the design be connected to the pad frame and then final simulation and design rule checks performed on the complete design. After that, the design was submitted for fabrication. Any minor error can cause the failure of the final fabricated chip at which stage it is impossible to perform any modification. Therefore, before our designs were submitted for fabrication, many simulations, design rule checks and some other checks (e.g. pad continuity checks) were performed.

Testing of the SOC Monitor Chip

The SOC monitor chip was fabricated through the MOSIS clearinghouse, located at the Univ. of Southern California [10], and is in the process of being tested. A special printed circuit board (PCB) was designed to test the SOC monitor chip. Eight light emitting diodes (LEDs) are installed on the PCB, and connected to one output port of the SOC monitor chip. By this means, all the test results or the intermediate data can be easily shown so that the running of a command or a program may be conveniently observed. The test procedure for the SOC monitor chip is shown in Fig. 5. To test a program on the SOC monitor chip, to avoid having to write the program in machine code, assembly language instructions were developed for the various commands and a compiler written to translate the assembly language instructions to machine code. The program memory has been implemented in an external UV EPROM into which the program can be burned. At present, only one command, the immediate transfer command has been tested. This command was found to work successfully. The testing of other commands is still in progress and additional test results on the SOC monitor IC chip will be presented at the conference.

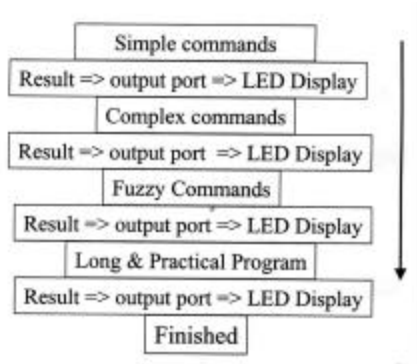


Figure 5 SOC Monitor IC Chip Test Procedure

Conclusion

In this paper, a coulomb-counting, fuzzy logic-based IC design for a smart battery SOC monitor for automotive batteries has been presented. The design and implementation of this SOC monitor chip has been presented. All the simulations for the functional level, gate level and transistor level have been completed successfully. The monitor chip has also been fabricated in 0.5 μm CMOS technology and a simple command has been successfully tested. Because of the inclusion of special fuzzy logic commands, a reduced program memory size can be achieved and the speed of the fuzzy logic algorithm can be higher than without these special commands.

After all the command tests are completed, the next step in this project is to add some additional functions, to the design including a controller area network (CAN) interface and a watchdog function. One standard data communication network used in vehicles is the CAN network. Therefore, incorporating the CAN interface will allow our smart battery controller chip to easily interface to a vehicle distributed sensor network. The watchdog feature can be used to reset the SOC monitor chip if there is some malfunction of the monitor IC.

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